means for direct memory access translation between the host computer and the hardware device;

means for supplying power to the hardware device; and

means for translating the timing between the host computer and the hardware device such that the host computer and the hardware device are interfaced and the functions of the hardware device are provided to the host computer.

2. (Amended) A system as defined in claim 1 wherein the first standard is the [a] PCMCIA standard and wherein the second standard is the [an] ISA standard.

3. (Amended) A system as defined in claim 1 wherein the first standard is the [a] PCMCIA standard and wherein the second standard is the [a] PCI standard.

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11. (Amended) A system for providing translation between a host computer having a first port, the first port compliant with a first standard, the first standard being selected from the group consisting of PCMCIA and CardBus, and a hardware device which is compliant with a second standard, the second standard being selected from the group consisting of ISA and PCI, the first standard and the second standard being non-compatible with each other and the hardware device requiring support for a plurality of interrupts, the system comprising:

means for interrupt translation between the host computer and the hardware device and for providing interrupt support for a plurality of interrupt request levels;

means for supplying power to the hardware device; and

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means for translating the timing between the host computer and the hardware device such that the host computer and the hardware device are interfaced and the functions of the hardware device are provided to the host computer.

12. (Amended) A system as defined in claim 11 wherein the first standard is the [a] PCMCIA standard and wherein the second standard is the [an] ISA standard.

13. (Amended) A system as defined in claim 11 wherein the first standard is the [a] PCMCIA standard and wherein the second standard is the [a] PCI standard.

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28. (Amended) A method for providing translation between a host computer having a first port, the first port compliant with a first standard, the first standard being selected ~~fro mthe~~ from the group consisting of PCMCIA and CardBus, and a hardware device which is compliant with a second standard, the second standard being selected from the group consisting of ISA and PCI, the first standard and the second standard being non-compatible with each other and the hardware device requiring support for a plurality of interrupts, the method comprising the steps of:

translating between the interrupts of the host computer and the plurality of interrupts of the hardware device;

supplying power to the hardware device; and

translating the timing between the host computer and the hardware device such that the host computer and the hardware device are interfaced and the functions of the hardware device are provided to the host computer.

29. (Amended) A method for providing translation between a host computer having a first port, the first port compliant with a first standard, the first standard being selected from the group consisting of PCMCIA and CardBus, and a hardware device which is compliant with a second standard, the second standard being selected from the group consisting of ISA and PCI, the first standard and the second standard being non-compatible with each other, the method comprising the steps of:

direct memory access translation between the host computer and the hardware device;

supplying power to the hardware device; and

translating the timing between the host computer and the hardware device such that the host computer and the hardware device are interfaced and the functions of the hardware device are provided to the host computer.

31. A system for providing translation between a host computer having a first port, the first port compliant with a first standard, and an 8 bit hardware device which is compliant with a second standard and a 16 bit hardware device which is compliant with the second standard, the first standard and the second standard being non-compatible with each other and the 8 bit and 16 bit hardware devices, the system comprising:

means for interrupt translation between the host computer and the 8 bit hardware device and the 16 bit hardware device, the 8 bit hardware device and the 16 bit hardware device being simultaneously connected to the first port of the computer;

means for supplying power to the 8 bit hardware device and the 16 bit hardware device; and

means for translating the timing between the host computer and the 8 bit hardware device and the 16 bit hardware device such that the both the 8 bit hardware device and the 16 bit hardware device are simultaneously connected to the host computer and the 8 bit hardware device and the 16 bit hardware device are interfaced and the functions of both of the hardware devices are provided to the host computer.

32. A system as defined in claim 31 wherein the first standard is a PCMCIA standard and wherein the second standard is an ISA standard.

33. A system as defined in claim 31 wherein the first standard is a PCMCIA standard and wherein the second standard is a PCI standard.

34. A system as defined in claim 31 wherein the means for interrupt translation comprises means for translating multiple interrupts required by the hardware device to a single interrupt.

35. A system as defined in claim 34 wherein the multiple interrupts comprises at least five interrupts.

36. A system as defined in claim 31 wherein the hardware device comprises at least one ISA compliant add-on circuit card.

37. A system as defined in claim 31 wherein the hardware device comprises at least one PCI compliant add-on circuit card.

38. A system as defined in claim 31 further comprising means for direct memory access translation.

39. A system as defined in claim 31 wherein the means for supplying power to the hardware device comprises:

means for supplying +12 volts;

means for supplying -12 volts;

means for supplying +5 volts; and

means for supplying -5 volts;

all at a current required to operate the 8 bit hardware device.

40. A system as defined in claim 31 wherein the port comprises a PCMCIA socket.

41. A system as defined in claim 31 wherein the means for translating the timing comprises a read/write timing generator.